NASA TECHNICAL MEMORANDUM

NASA TM X-2442

NASA TM X-2442

SILICON-CONTROLLED-RECTIFIER SQUARE-WAVE INVERTER WITH PROTECTION AGAINST COMMUTATION FAILURE

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NATIONAL AERONAUTICS AND SPACE ADMINISTRATION • WASHINGTON, D. C. • DECEMBER 1971

1. Report No.	2. Government Accession No.	3. Recipient's Catalog No.
NASA TM X-2442		

4. Title and Subtitle	5. Report Date
SILICON-CONTROLLED-RECTIFIER SQUARE-WAVE INVERTER WITH PROTECTION AGAINST COMMUTATION FAILURE	December 1971
	6. Performing Organization Code
7. Author(s)	8. Performing Organization Report No.
Arthur G. Birchenough	E-6528
	10. Work Unit No.
9. Performing Organization Name and Address	112-27
Lewis Research Center National Aeronautics and Space Administration Cleveland, Ohio 44135	11. Contract or Grant No.
	13. Type of Report and Period Covered
12. Sponsoring Agency Name and Address	Technical Memorandum
National Aeronautics and Space Administration Washington, D.C. 20546	14. Sponsoring Agency Code

15. Supplementary Notes

16. Abstract

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17. Key Words (Suggested by Author(s))	18. Distribution Statement
SCR Inverter Forced commutation Commutation failure protection	Unclassified - unlimited

19. Security Classif. (of this report)	20. Security Classif. (of this page)	21. No. of Pages	22. Price*
Unclassified	Unclassified	22	$3.00

* For sale by the National Technical Information Service, Springfield, Virginia 22151

SILICON-CONTROLLED-RECTIFIER SQUARE-WAVE INVERTER WITH PROTECTION AGAINST COMMUTATION FAILURE

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SUMMARY

A square-wave silicon controlled rectifier inverter that was designed, built, and tested includes a circuit to turn off the inverter in case of commutation failure. The basic power stage is a complementary impulse-commutated parallel inverter consisting of only six components. The 400-watt breadboard was tested while operating at ±28 volts, and it had a peak efficiency of 95.5 percent at 60 hertz and 91.7 percent at 400 hertz. The voltage regulation for a fixed input was 3 percent at 60 hertz. An analysis of the operation and design information is included.

INTRODUCTION

A technique under consideration for starting dynamic space-power systems involves using the alternator as a motor to accelerate the rotating assembly to the speed at which it becomes self-sustaining (refs. 1 and 2). In the 2- to 15-electrical-kilowatt (kW_e) Brayton space-power system under investigation at the NASA-Lewis Research Center, the inverter, which drives the alternator, is required to supply a peak output current of nearly 200 amperes. A transistor inverter was designed and built for this application; however, because higher-current - higher-voltage silicon controlled rectifiers (SCR's) are more available, SCR-inverters are generally more practical, particularly on larger systems.

A major disadvantage of dc-ac SCR inverters, however, is the possibility that an SCR will not commutate. A commutation failure generally results in a low-impedance short across the dc supply. In general, the commutation circuit also requires a significant number of additional parts. The inverter described in this report requires only six parts in the power stage, including the two components required for commutation. A

modification that will turn off the inverter in case of a commutation failure, clearing the short circuit on the input lines, is also discussed.

Current and voltage transients are inherently limited, without the use of di/dt or dv/dt snubbers, and the circuit is basically frequency and symmetry independent. A 400-watt, 400-hertz, single-phase model powered from a ±28-volt source was designed and tested for this investigation.

CIRCUIT DESCRIPTION

Power Stage Operation

As in most square-wave inverters, this design consists primarily of a pair of switches, SCR1 and SCR2 (fig. 1), that alternately connect the load to opposite terminals of the power supply. Although the center tapped inductor L and C_8 form a low pass filter, they are too small to provide any substantial filtering; their function is in the commutation of the SCR's. Figure 2 shows the ideal waveforms for one cycle of operation. At t_1 in figure 2, SCR1 is conducting. There is a current i_L in one winding of L and in the load, and C_8 is charged to nearly V+. The commutation cycle is started by firing SCR2, which conducts, connecting terminal 3 of L to V-. Because C is charged to V+, there will be a voltage of 2V across the winding between terminals 2 and 3 of L. The turns ratio of L is 1:1, so a voltage of 2V will be induced in the other winding. This reverse biases SCR2, to a voltage of -2V, turning it off. The capacitor C_8 is now supplying the load current and the current that was flowing in L equal to the

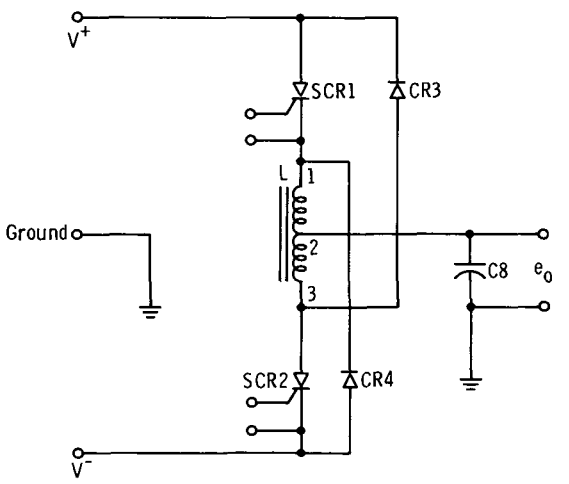


Figure 1. - Basic inverter power stage.

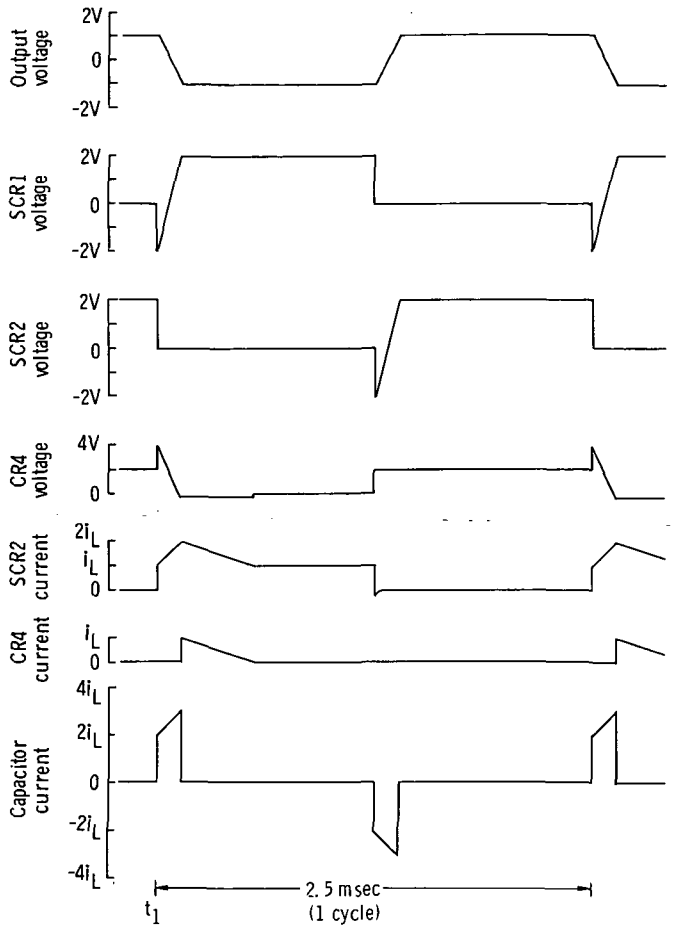


Figure 2. - Ideal waveforms.

load current i_L. This current is now flowing in the winding between terminals 2 and 3 of L through SCR2, since SCR1 is off. Capacator C_8 also supplies the increasing current in L due to the voltage across it. As C_8 discharges to 0, SCR1 is no longer reverse biased, but it will have regained its forward blocking ability.

When C_8 charges to V-, the commutation cycle is ended, but the excess current that built up in L during commutation must be dissipated. This current will circulate through CR4 and SCR2 until the energy is dissipated in the semiconductor and I R losses. At this time SCR1 can be tripped and the cycle repeated. The time scale has been distorted in figure 2 to show the operation more clearly. The time required for commutation is 15 microseconds. It should be noted that the peak forward or reverse SCR voltage is only 2V and the dv/dt is limited by C_8. The di/dt is limited by the SCR turnon characteristics until the current reaches i_L, and then the di/dt is limited by L. Even the diode stress is limited to 4V. The peak voltage, peak current, and dv/dt and di/dt

stresses are very low, and the turnoff time of the SCR, which is highly reverse biased during turnoff, is the only critical parameter. The load capability of the inverter is very near the 180° conduction current rating of the SCR's.

The size of the commutation components can be found from the equation for the output voltage during the commutation internal, obtained in appendix A:

$$e(t) = 2e_0 \cos \frac{t}{\sqrt{LC}} - 2i_L \sqrt{\frac{L}{C}} \sin \frac{t}{\sqrt{LC}} - e_0$$

where

$e(t)$	output voltage
e_0	output voltage at start of commutation
L	inductance of one winding of commutation inductor L
C	capacitance of commutation capacitor C_8
i_L	load current

This equation assumes that i_L is constant during the commutation cycle, as with an inductive load, which is the worst case. Full load gives the shortest commutation time, and, since $t \ll LC$, using the approximation $\sin w \approx w$ and $\cos w \approx 1 - w^2/2$ results in

$$e(t) \approx e_0 - 2i_L \frac{t}{c} - \frac{t^2}{LC} e_0$$

To find the capacitor size, set $e(t) = 0$, for at this time the SCR is no longer reverse biased.

$$C \approx \frac{2i_L t}{e_0} + \frac{t^2}{L}$$

Using the maximum value of the SCR parameter "t off" for t gives the minimum value for C.

Practical values for L have only a second-order effect on C, and L is selected for acceptable physical size and peak SCR current.

The current in the capacitor is simply

$$i = C\frac{de_0}{dt}$$

and the rms current is approximately

$$I_{rms} = (E_{0,rms})(2\pi fC)$$

where f is the output frequency. This current is less than 1 ampere for this inverter and allows the use of high-density metalized or electrolytic capacitors.

The operation of this circuit is very similar to a form of a Bedford-McMurray inverter (refs. 3 and 4). The primary difference is the placement of the diodes. This placement improves the waveshape and reduces the peak reverse voltage on the SCR's.

Turnoff Modification

As a single-phase inverter, this circuit has the disadvantage that it cannot be turned off under load, because turning off one SCR is accomplished by turning on the other. With no load, the circuit can be turned off by simply discontinuing the firing pulses because the SCR current decreases to zero as the commutation energy is dissipated. For a three-phase inverter with a delta-connected load, turnoff can be accomplished by discontinuing all firing pulses to the three SCR's connected to either input bus. The load current then ceases, and the other SCR's turn off.

Single-phase turnoff can be accomplished under load with the addition of the components shown within the dashed lines of figure 3. The turnoff is initiated by firing SCR3 and discontinuing all pulses to SCR1 and SCR2. The capacitor C_7 is discharged, so a voltage of 2V will be applied to the additional winding on L. This voltage is transformed across to the other windings, and the load SCR's will both be reverse biased and commutate. The turns ratio from the primary (the added winding) to the total secondary must be greater than 1:1 to reverse bias both SCR's. A ratio of 2:1 was used in this inverter. Capacitor C_7 is sized using the same equation as for C_8. When C_7 charges to 2V, SCR3 commutates and R_{15} discharges C_7. This circuit increases the nonrepetitive reverse voltage across the load SCR's. Commutation failure protection is provided by sensing the failure, as described later, and firing this turnoff circuit.

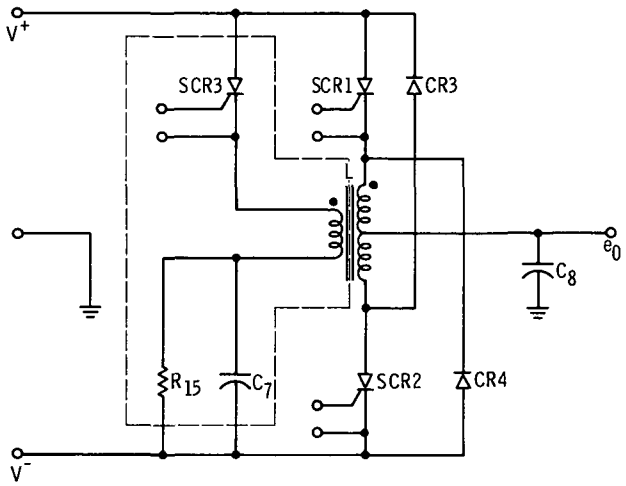


Figure 3. - Turnoff circuit.

Commutation Energy Return

The additions of figure 4 provide a path for the commutation energy stored in L to return to the supply. While the commutation energy is being dissipated, there will be a voltage across L, as indicated in figure 4, equal to the forward drops of the SCR and diode circulating the current. The voltage is reflected to the additional winding, and commutation current will flow in the secondary through CR4 to the supply if the turns ratio is greater than

$$\frac{2V}{V_{SCR} + V_{DIODE}}$$

where V is the supply voltage and V_{SCR} and V_{DIODE} are the forward voltage drops of the semiconductors. The diode voltage and current are shown in figure 5, where t_1 corresponds to t_1 in figure 2. The current in the load SCR changes from that shown in figure 2, and the diodes in the original circuit will carry no current unless the load is inductive. This circuit was not used during performance testing. The turns ratio necessary to achieve satisfactory energy return reduces the maximum operating frequency because the inductor discharges more slowly and induces very large reverse voltages on CR5. Also, the large number of secondary turns introduces stray capacitance effects in the inductor.

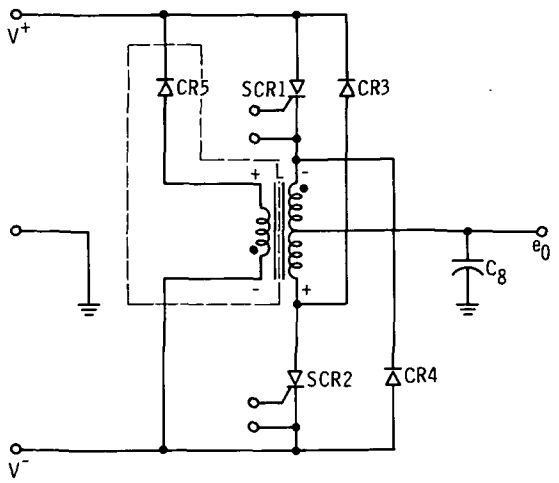


Figure 4. - Commutation energy return circuit.

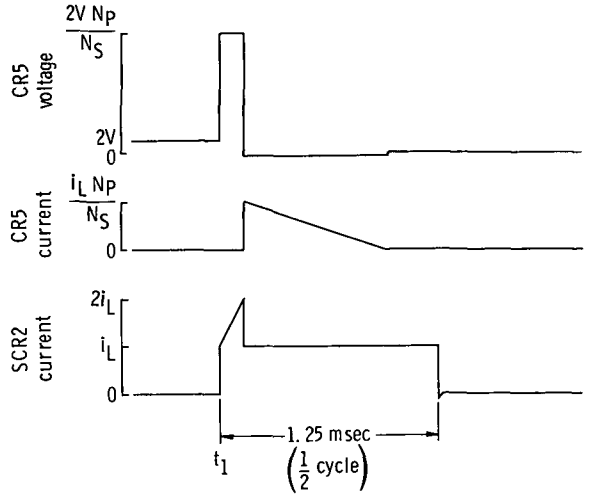


Figure 5. - Commutation energy return circuit waveforms. (N_P/N_S = turn ratio.)

Control Circuits

Because there are no critical timing problems in this inverter, there are almost no restrictions on the firing pulses. An SCR must not be fired while it is being commutated, or the commutation cycle may fail: The two SCR's would be on, and the supply would be short circuited. Also, if the SCR's are fired at too high a frequency, before the commutation energy is removed from the inductor, the inductor may saturate and the inverter will fail to commutate. The maximum frequency of this inverter was approximately 1000 hertz. These restrictions are the only limits on the operating frequency of the inverter

or on the firing pulses. The timing of the firing pulses to the two SCR's need not be symmetrical if a nonsymmetrical output is desired; pulsing a SCR while in conduction normally has no effect, so the pulses need not be alternated. It is generally advisable to supply a string of pulses to the SCR in case the SCR current has temporarily fallen below the holding current, as with inductive or light loads.

The control circuit used for the inverter is shown in figure 6. Operational amplifier IC1 is used as a square wave oscillator, operating at twice the inverter output frequency, followed by a buffer IC2A and a flip-flop, IC3A. The outputs of IC3A are two 180° out-of-phase symmetrical square waves at the inverter output frequency. Inverters IC2B, IC2C, and IC2D form a second oscillator that generates 5-microsecond pulses at a 50-microsecond repetition rate. This oscillator is gated on during the first half of each cycle by IC1. These pulses and the flip-flop outputs are NANDed together in IC4A and IC4B to produce the SCR drive pulses.

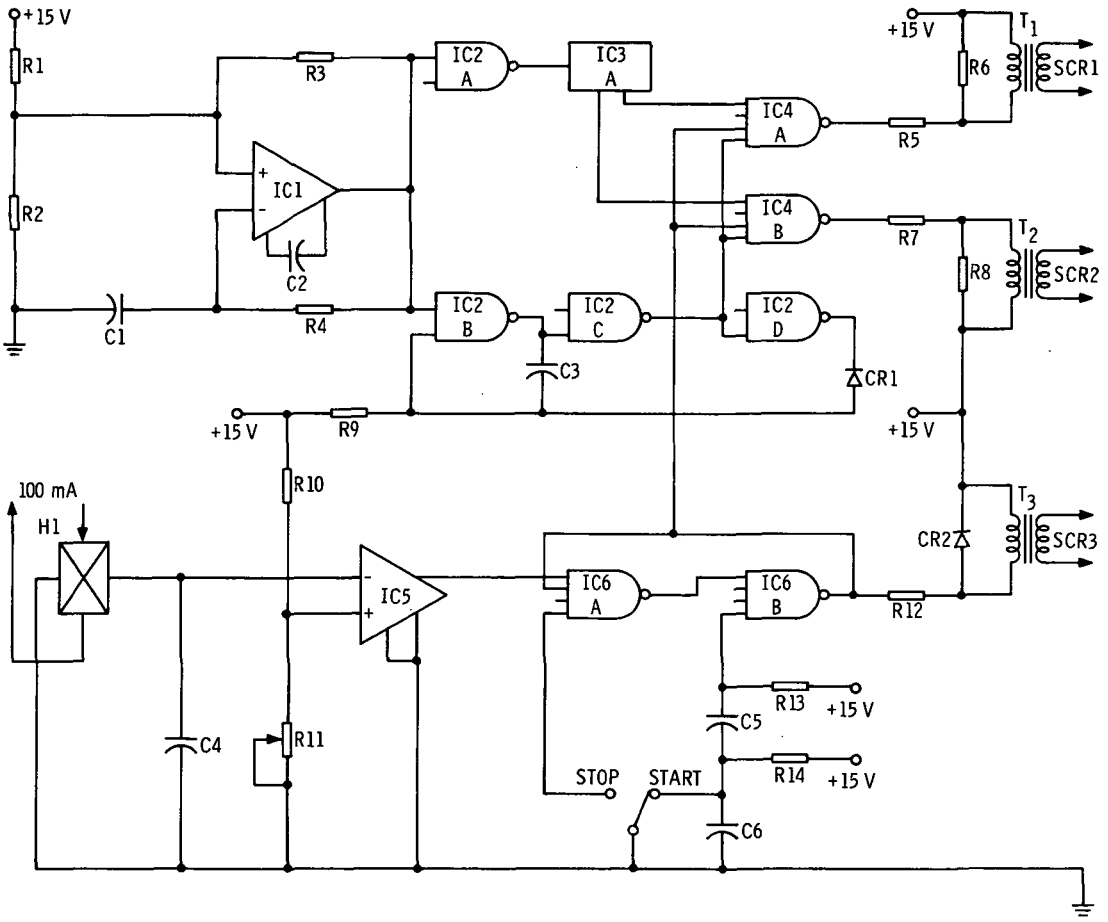


Figure 6. - Control circuit.

Also shown in figure 6 is the circuit used to control the turnoff in case of a commutation failure. Inverter IC5 senses the output of a Hall effect device located in the commutation inductor. The output voltage of the Hall device is proportional to the core flux, which increases if the circuit fails to commutate. If the flux rises above the set point, IC5 trips a latch, IC6, turning off the power stage firing pulses and firing SCR3. A start-stop switch that manually controls IC6 is included.

RESULTS AND DISCUSSION

The single-phase version of the inverter built and tested for this investigation is shown in figure 7. As shown, the SCR's and diodes of the power circuit are mounted on the heat sinks. Two commutation capacitors, in parallel, were used to obtain the correct value. The additions to the power stage for turnoff are not shown. (This additional SCR would not require any heat sinking.) A complete schematic (fig. 18) and parts list are in appendix B.

Waveshape

Waveforms of the inverter operating at 400-hertz, ±30-volt input, and full load (1.5

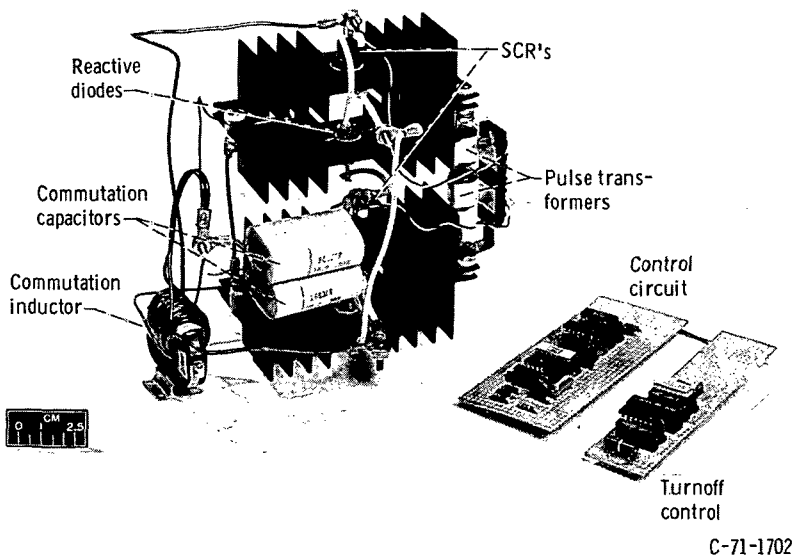


Figure 7. - Breadboard inverter power stage and control circuit.

ohms with a small series inductive component) are shown in figures 8 to 12. The output voltage (fig. 8) shows a slight ringing at each switching. This ringing is reflected in the voltage and can be reduced with an input filter. The voltage change approximately halfway through each half-cycle indicates the end of the commutation energy dissipation cycle.

The SCR voltage is shown in figure 9, and an expanded time picture of the commutation spike in figure 10. The peak voltage from these figures is approximately twice the supply voltage, and the maximum dv/dt is about 4 volts per microsecond.

The SCR current shown in figure 11 shows a large spike during the recovery time of the SCR being commutated and the current decay as the commutation energy is dissipated.

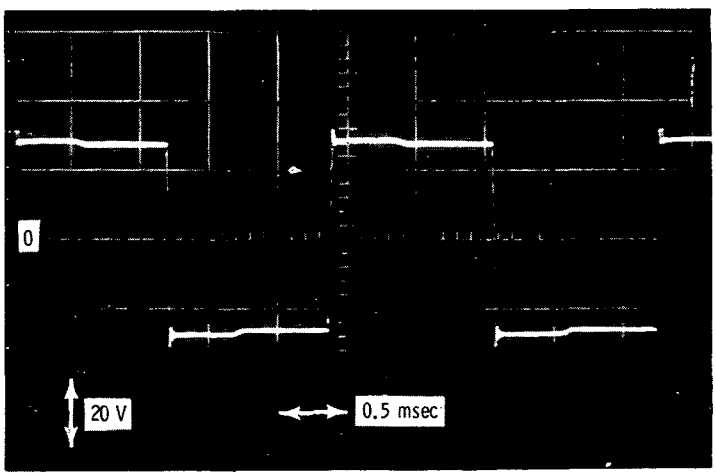


Figure 8. - Inverter output voltage.

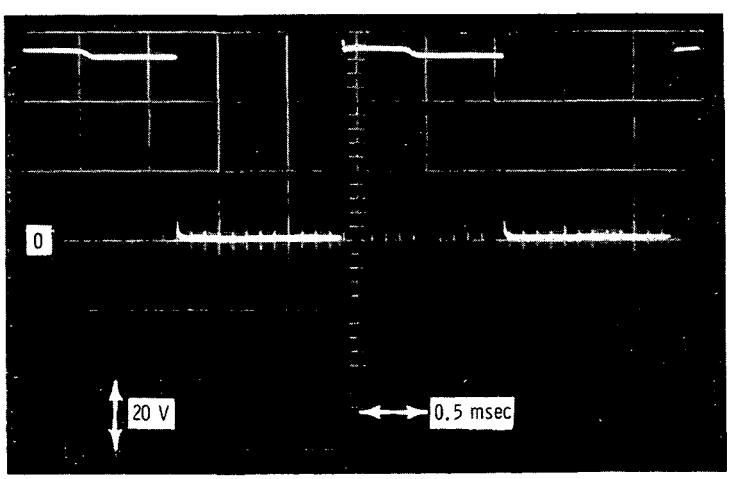


Figure 9. - SCR anode voltage.

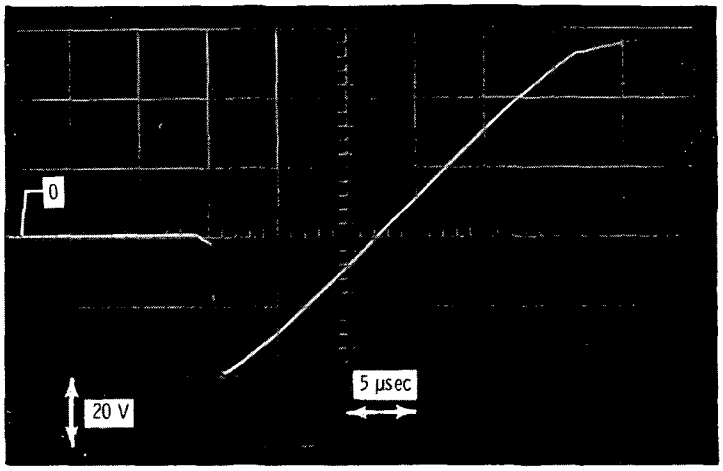


Figure 10. - SCR anode voltage during commutation.

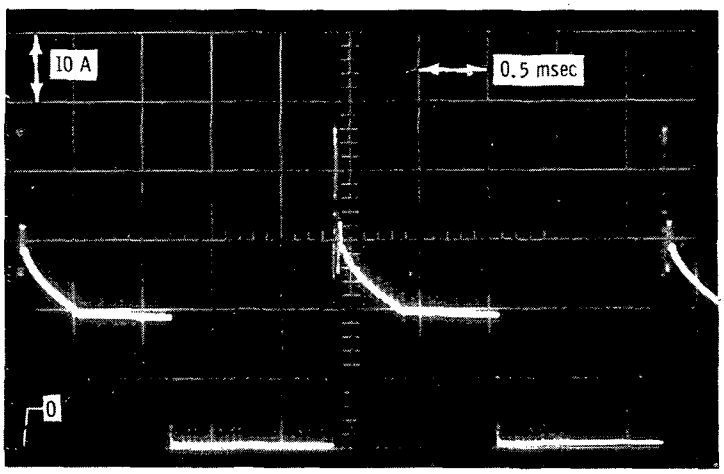


Figure 11. - SCR anode current.

The SCR current at turn-on is shown in figure 12. The current, limited by the SCR turn-on time characteristics, rises almost instantly to the load current, and then increases by approximately 1 ampere per microsecond. The SCR-limited current rise to approximately the rms rating of the SCR is within the di/dt rating of most inverter SCR's.

Efficiency

The efficiency of the inverter was measured at 400, 200, and 60 hertz and over a supply voltage range of ±15 to ±30 volts. The load was resistive, although the wattmeter

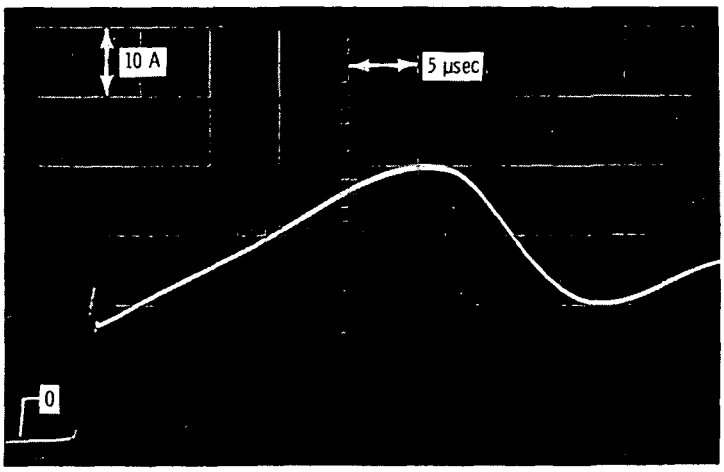
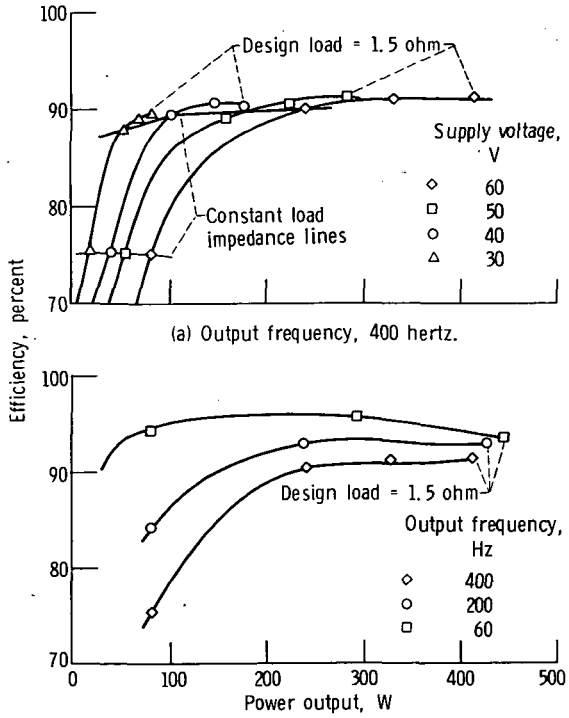


Figure 12. - SCR anode current at turn-on.

added a slight inductive component. The power factor was approximately 0.9 at the worst case of 400 hertz full load. Figure 13(a) shows the efficiency at 400 hertz for varying load and input voltage. The efficiency was nearly independent of voltage for a fixed load impedance because the power output and the major loss (commutation energy) are both proportional to the input voltage squared. Figure 13(b) shows the effect of frequency on the efficiency. Commutation energy is constant each cycle and is therefore proportional to frequency and independent of load. Since the commutation energy is a major loss, the efficiency decreases at low output powers and higher frequency. The peak measured efficiency was 95.5 percent at 60 hertz for a 294-watt output and 91.7 percent at 400 hertz for a 415-watt output.

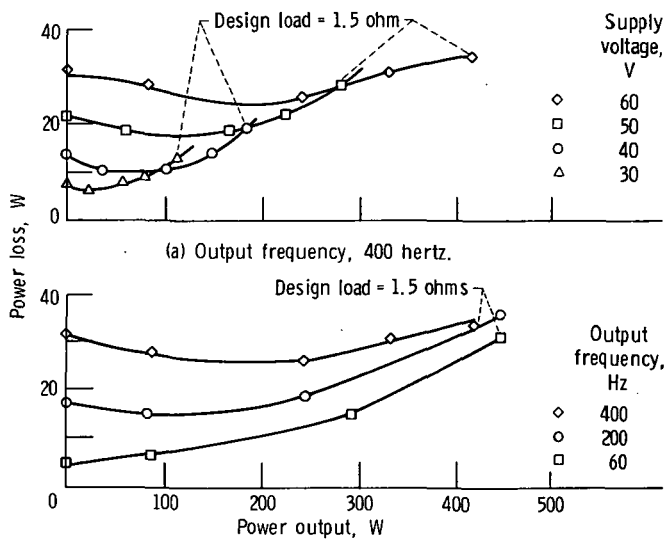
The power loss for the same conditions is shown in figure 14. The total loss is lower at light loading than at no load because some of the commutation energy is delivered to the load. At 60 hertz, this effect has disappeared because commutation energy is no longer the major loss. The loss curves become asymptotic to a line through the origin at high powers, which indicates that the major loss is the constant voltage drop of the SCR's. Higher voltage inverters would then tend to be more efficient (see fig. 13) because the SCR drop would be almost constant.

The output voltage is proportional to the supply voltage and drops with load (fig. 15). At no load, the output voltage is completely flat as shown in figure 16. With a load, the voltage drop of the SCR produces the notch approximately halfway through each half cycle (see fig. 8). At 60 hertz, the loading effect of the wattmeter was great enough to generate this notch, which accounted for the lower no-load output voltage at 60 hertz. The regulation from no load to full load at 60 hertz and ±30 volts input was 3 percent.



(b) Supply voltage, 50 volts.

Figure 13. - Inverter efficiency characteristics.



(b) Supply voltage, 60 volts.

Figure 14. - Inverter power dissapation.

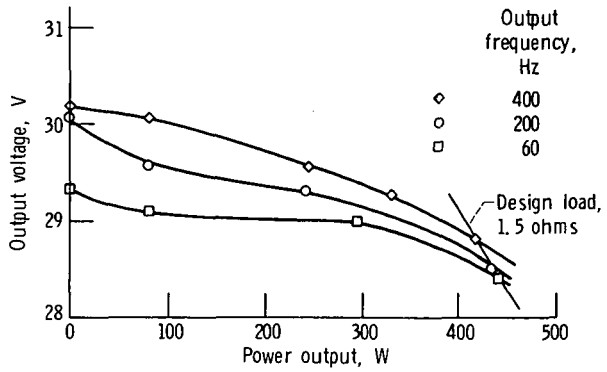


Figure 15. - Output voltage characteristic. Supply voltage, 60 volts.

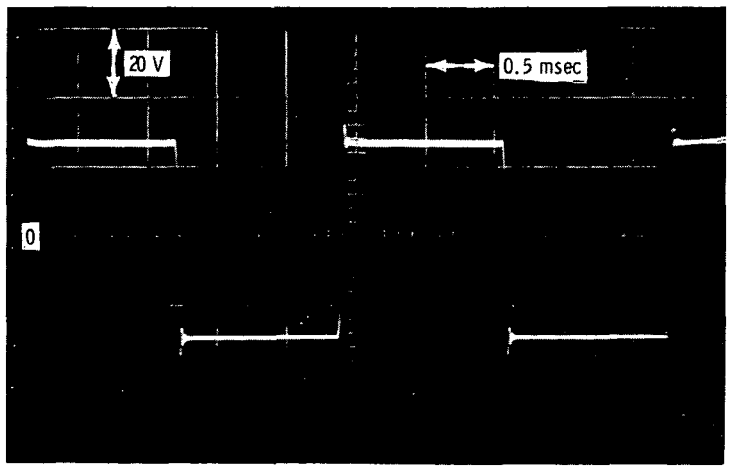


Figure 16. - No-load output voltage.

The turnoff circuit was able to turn off the inverter from any normal operating condition. Use of this circuit requires an increase in the volt-second capacity of the core so that the inductor does not saturate if turnoff is attempted during or immediately following a normal commutation or a commutation failure. Successful turnoff was accomplished with a transient up to 3 times rated load. The maximum transient load that can be successfully turned off is determined by the size of C_7.

CONCLUDING REMARKS

A breadboard impulse-commutated SCR inverter requiring only six components in the output stage was built and tested. The circuit has no frequency or symmetry limits

except a minimum pulse width, which also limits the maximum frequency to approximately 1000 hertz.

With the addition of a turnoff circuit and a flux or overcurrent detector, overloads or other conditions producing a commutation failure result in only a turnoff of the inverter instead of an input-bus short.

The components are operated at very low peak voltages, currents, and low rates of rise of voltage and current, dv/dt and di/dt without the use of snubbers. Also, the maximum load current rating of the inverter is approximately the 180^{o} conduction rating of the SCR's.

The 400-watt test inverter was operated over a range of frequency from 60 to 400 hertz with input voltages from ±15 to ±30 volts. The peak efficiency was 95.5 percent.

Lewis Research Center,
National Aeronautics and Space Administration,
Cleveland, Ohio, September 29, 1971,
112-27.

APPENDIX A

The equations describing the commutation internal are based on these assumptions:

(1) The elements are ideal and lossless.

(2) The output voltage e_0 just before commutation is equal to V the supply voltage.

(3) The load current i_L is constant during the commutation interval.

This is the worst case and approximates an inductive load. The equivalent circuit used for the analysis is shown in figure 17

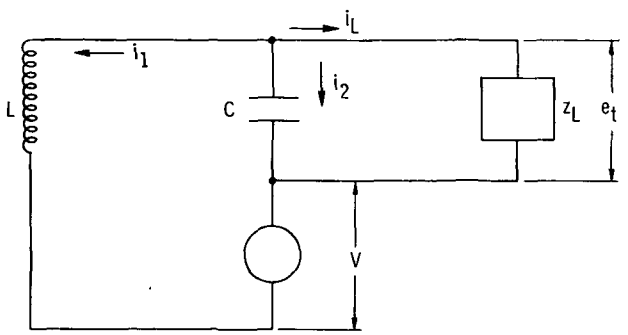


Figure 17. - Equivalent circuit.

where L is one winding of the commutation inductor, V is the supply voltage, C is the commutation capacitor, and z_L and i_L are the load impedance and current.

$$i_1 + i_2 + i_L = 0 \tag{1}$$

$$e(t) + V = L \frac{di_1}{dt} \tag{2}$$

$$e(t) = e_0 + \frac{1}{C} \int_0^t i_2 \, dt \tag{3}$$

$$e_0 = V \text{ (assumption (2))}$$

Combining equations (2) and (3) results in

$$L \frac{di_1}{dt} = 2e_0 + \frac{1}{C} \int_0^t i_2 \, dt \tag{4}$$

Combining equations (1) and (4) result in

$$L \frac{di_1}{dt} = 2e_0 - \frac{1}{C} \int_0^t (i_1 + i_L) \, dt$$

$$L \frac{di_1^2}{dt^2} = - \frac{1}{C} (i_1 + i_L)$$

$$\frac{di_1^2}{dt^2} = - \frac{1}{LC} (i_1 + i_L) \tag{5}$$

The standard solution for equation (5) is

$$i_1 = A \sin \frac{t}{\sqrt{LC}} + B \cos \frac{t}{\sqrt{LC}} - i_L \tag{6}$$

At $t \approx 0$, $i_1 = i_L$ since the load current was flowing in the other winding of L just before the commutation internal. Therefore,

$$B = 2i_L$$

and

$$\frac{di_1}{dt} = \frac{A}{\sqrt{LC}} \cos \frac{t}{\sqrt{LC}} - \frac{B}{\sqrt{LC}} \sin \frac{t}{\sqrt{LC}} \tag{7}$$

From equations (2) and (7)

$$\left.\frac{di_1}{dt}\right|_{t=0} = \frac{2e_0}{L} = \frac{A}{\sqrt{LC}}$$

$$A = 2e_0\sqrt{\frac{C}{L}}$$

$$i_1 = 2e_0\sqrt{\frac{C}{L}}\sin\frac{t}{\sqrt{LC}} + 2i_L\cos\frac{t}{\sqrt{LC}} - i_L \qquad (8)$$

From equations (1) and (3)

$$e(t) = e_0 - \frac{1}{C}\int_0^t (i_1 + i_L)\,dt$$

Substituting i_1 from equation (8) and integrating result in

$$e(t) = 2e_0\cos\frac{t}{\sqrt{LC}} - 2i_L\sqrt{\frac{L}{C}}\sin\frac{t}{\sqrt{LC}} - e_0$$

APPENDIX B

PARTS LIST AND SCHEMATIC

Part		Part	
$R_1 R_2$	47 K	IC1	μA 748
R_3	33 K	IC2	MC672
R_4	8.2 K	IC3	MC663
R_5, R_7	180	IC4, IC6	MC679
R_6, R_8	1 K	IC5	LM311D
R_9, R_{10}, R_{13}	15 K	CR1, CR2	IN459
R_{11}	1 K potentiometer	CR3, CR4	IN3891
R_{12}	220, 1 W	SCR1, SCR2	C40A
R_{14}	150 K	SCR3	C30D
R_{15}	1 K, 1 W	T_1, T_2, T_3	1:1 ratio pulse transformer
C_1	0.05	L	Commutation inductor AL-8 core, 20-mil gap winding 1-2, 12 turns winding 2-3, 12 turns winding 4-5, 6 turns
C_2	10 pF		
C_3	0.005		
C_4	0.47	H_1	Hall effect device H. W. Bell BH-700
C_5	0.0005		
C_6	0.01		
C_7	110 μF		
C_8	20 μF		

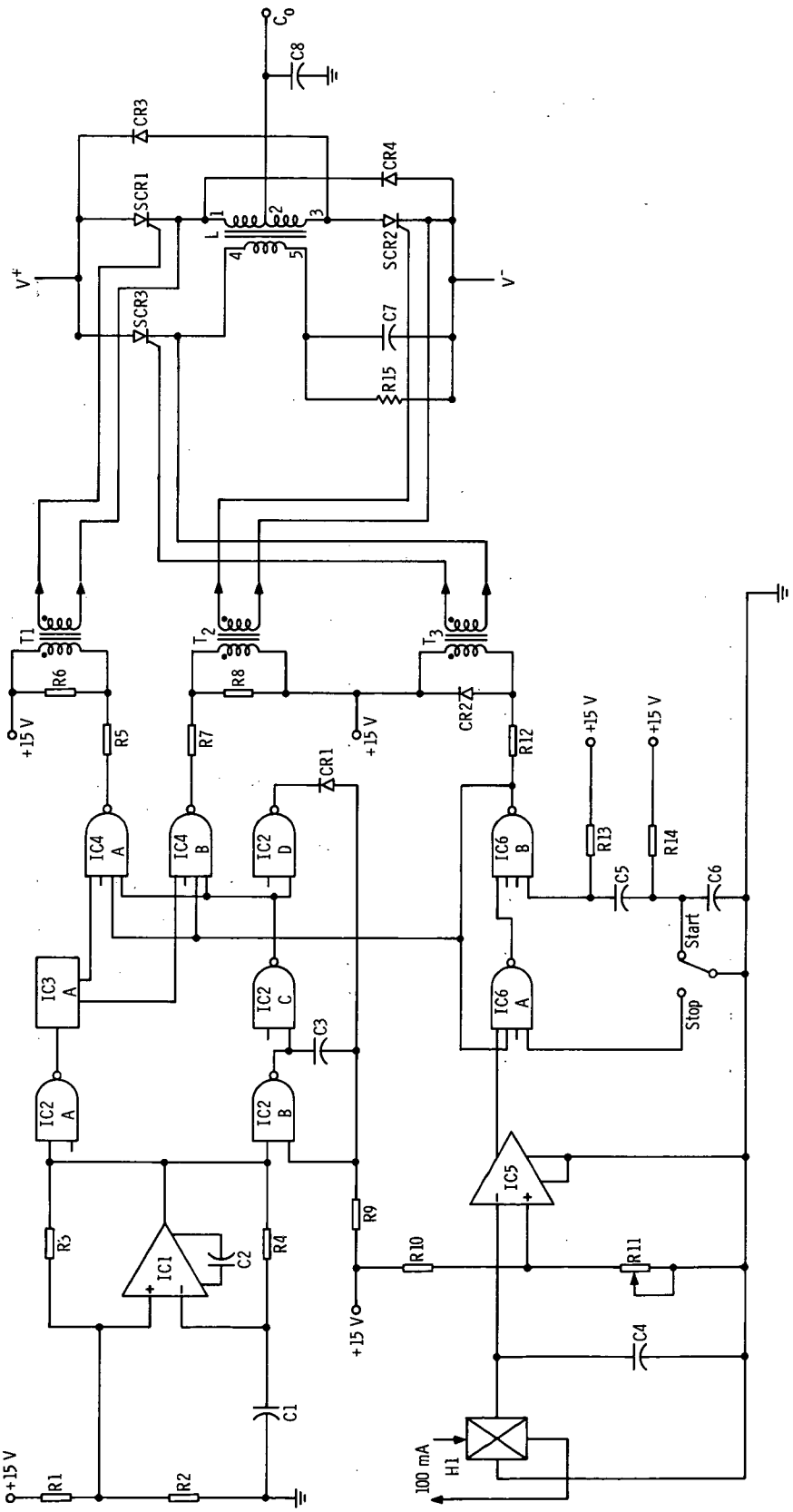


Figure 18. - Complete schematic of SCR inverter.

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